WHAT IS CLAIMED IS:

1. A memory repair method comprising the steps of:

providing an E-fuse farm storing memory repair information, and a memory module comprising associated memory module circuitry, power control logic and repair data registers;

powering up the E-fuse farm and the memory module, and loading the repair information into the memory module via the E-fuse farm during the power-up; and

maintaining power to the power control logic and repair data registers during loss of power to the E-fuse farm and associated memory module circuitry, such that the memory repair information is retained by the memory module during the loss of power to the E-fuse farm and associated memory module circuitry.

2. The method according to claim 1, wherein the step of maintaining power to the power control logic and repair data registers during loss of power to the E-fuse farm and associated memory module circuitry comprises maintaining power solely to data retention latch circuitry associated with the repair data registers.

3. The method according to claim 2, wherein the step of maintaining power to the power control logic and repair data registers during loss of power to the E-fuse farm and associated memory module circuitry further comprises generating memory module power control logic signals to isolate the retention latch circuitry before loss of power to the memory module.

4. The method according to claim 1, wherein the step of powering up the E-fuse farm and the memory module, and loading the repair information into the memory module via the E-fuse farm during the power-up comprises activating a Vdd header switch to provide power to the memory module.

5. The method according to claim 1, wherein the step of powering up the E-fuse farm and the memory module, and loading the repair information into the memory module via the E-fuse farm during the power-up comprises activating a Vss footer switch to provide power to the memory module.

6. A memory repair method comprising the steps of:

providing a device including an E-fuse farm storing memory repair information, and at least one memory module comprising associated memory module circuitry, power control logic and repair data registers;

powering up the device, and transferring the repair information into the memory module via the E-fuse farm during the power-up; and

maintaining power to the memory module power control logic and memory module repair data registers during loss of power to the E-fuse farm and associated memory module circuitry, such that the memory repair information is retained by the memory module during the loss of power to the E-fuse farm and associated memory module circuitry.

7. The method according to claim 6, wherein the step of maintaining power to the memory module power control logic and memory module repair data registers during loss of power to the E-fuse farm and associated memory module circuitry comprises maintaining power solely to data retention latch circuitry associated with the memory module repair data registers.

8. The method according to claim 7, wherein the step of maintaining power to the memory module power control logic and memory module repair data registers during loss of power to the E-fuse farm and associated memory module circuitry further comprises generating memory module power control logic signals to isolate the memory module retention latch circuitry before loss of power to the memory module circuitry.

9. The method according to claim 6, wherein the step of powering up the device, and transferring the repair information into the memory module via the E-fuse farm during the power-up comprises activating at least one Vdd header switch to provide power to the memory module.

10. The method according to claim 6, wherein the step of powering up the device, and transferring the repair information into the memory module via the E-fuse farm during the power-up comprises activating at least one Vss footer switch to provide power to the memory module.

11. A memory device with repair capability comprising:

a supply voltage;

power control logic connected to the supply voltage;

at least one switch connected to the supply voltage;

a memory array connected to the at least one switch;

peripheral logic connected to the at least one switch; and

repair data registers connected to the supply voltage and the at least one switch, wherein the at least one switch is operational to remove power to the peripheral logic, the memory array and selected portions of the repair data registers in response to power control logic signals such that memory repair data is retained in the repair data registers subsequent to power down of the peripheral logic, the memory array, and the selected portions of the repair data registers.

12. The memory device according to claim 11, wherein the repair data registers comprise retention latch circuitry operational to store and maintain the memory repair data.

14. A memory device with repair capability comprising:

a supply voltage;

power control logic connected to the supply voltage;

at least one switch selected from the group consisting of a Vss footer switch, and a Vdd header switch;

a memory array connected to the at least one switch;

peripheral logic connected to the at least one switch; and

repair data registers connected to the supply voltage and the at least one switch, wherein the at least one switch is operational to remove power to the peripheral logic, the memory array and selected portions of the repair data registers in response to power control logic signals such that memory repair data is retained in the repair data registers subsequent to power down of the peripheral logic, the memory array, and the selected portions of the repair data registers.

15. The memory device according to claim 14, wherein the repair data registers comprise retention latch circuitry operational to store and maintain the memory repair data.

16. A device with memory repair capability comprising:

power management control logic;

an E-fuse farm; and

at least one memory module comprising repair data registers, wherein the at least one memory module operates to maintain memory repair data in the repair data registers in response to power management control logic signals during loss of power to portions of the device.

17. The device according to claim 16, wherein the at least one memory module comprises:

a supply voltage;

power control logic connected to the supply voltage;

at least one switch selected from the group consisting of a Vss footer switch, and a Vdd header switch;

a memory array connected to the at least one switch;

peripheral logic connected to the at least one switch; and

repair data registers connected to the supply voltage and the at least one switch, wherein the at least one switch is operational to remove power to the peripheral logic, the memory array and selected portions of the repair data registers in response to power control logic signals such that memory repair data is retained in the repair data registers subsequent to power down of the peripheral logic, the memory array, and the selected portions of the repair data registers.

18. The device according to claim 16, wherein the repair data registers comprise retention latch circuitry operational to store and maintain the memory repair data.